

FIG. 3 PRIOR ART

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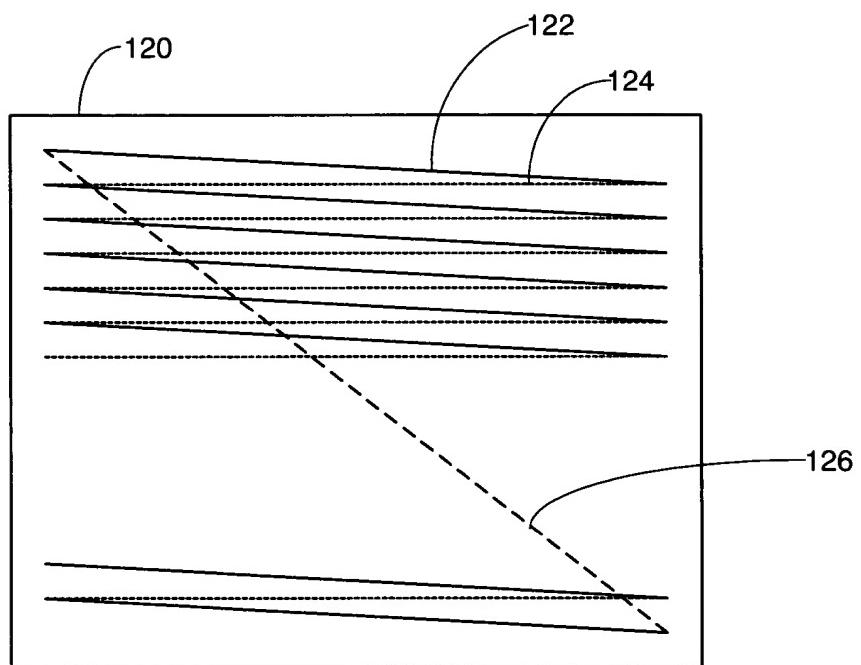


FIG. 4

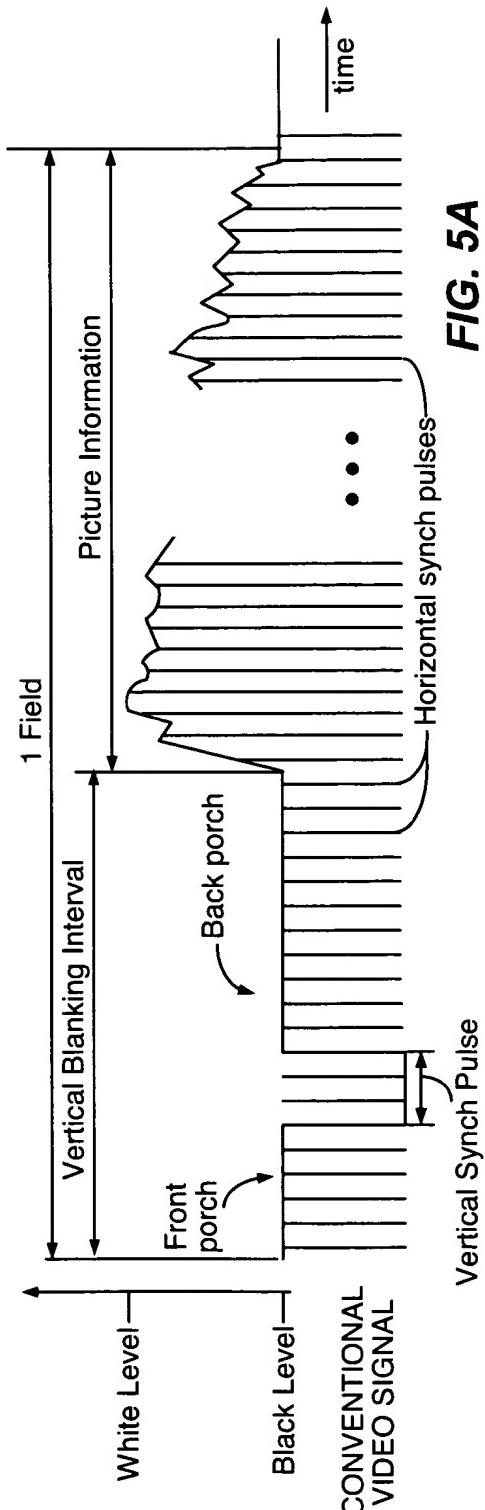


FIG. 5A

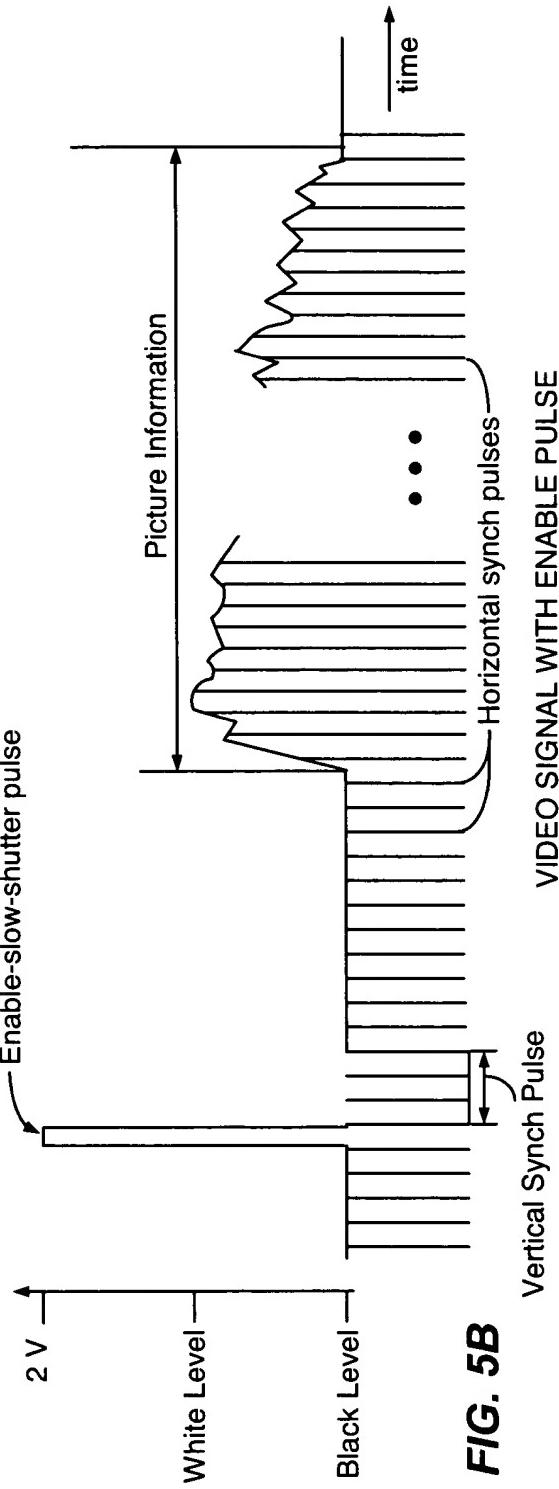
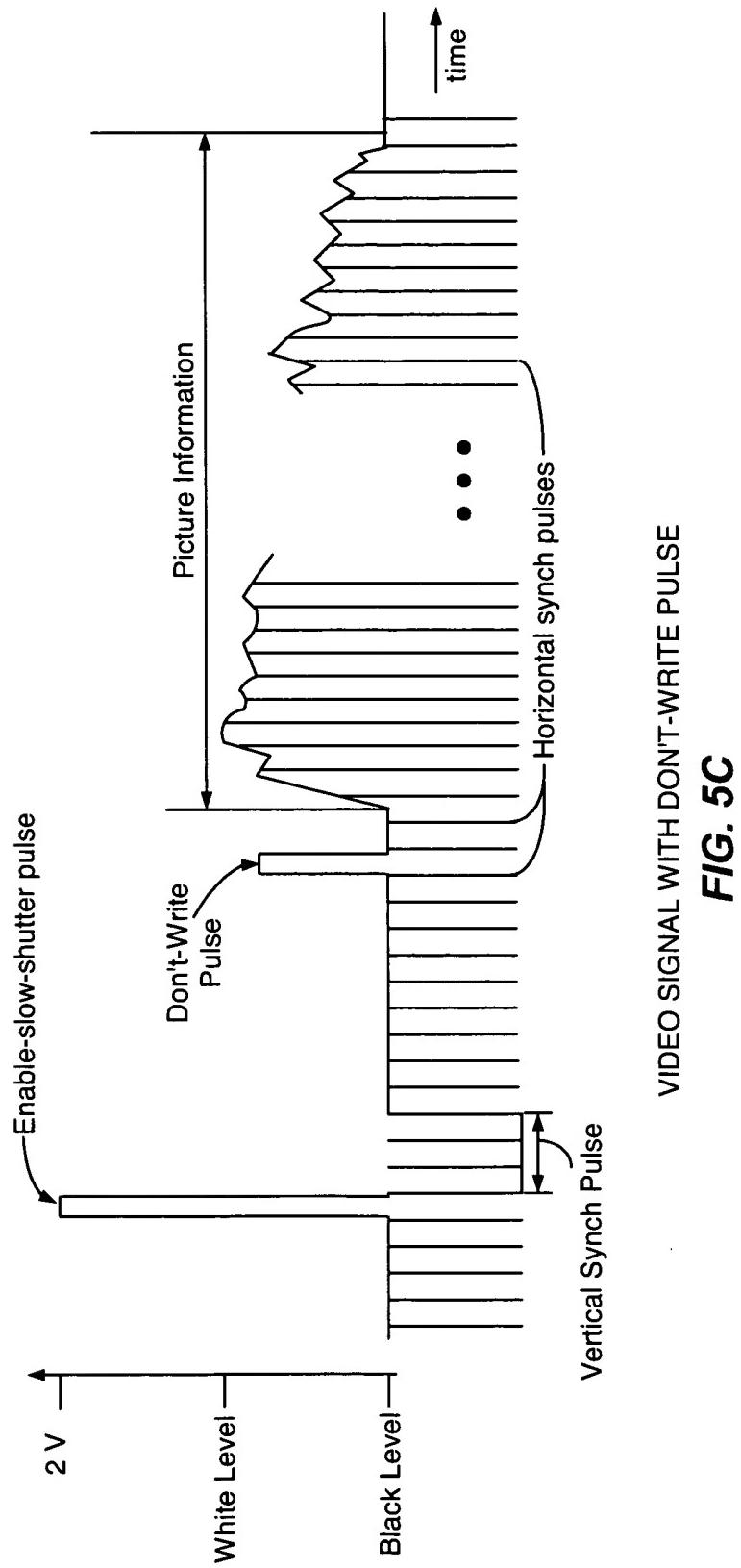
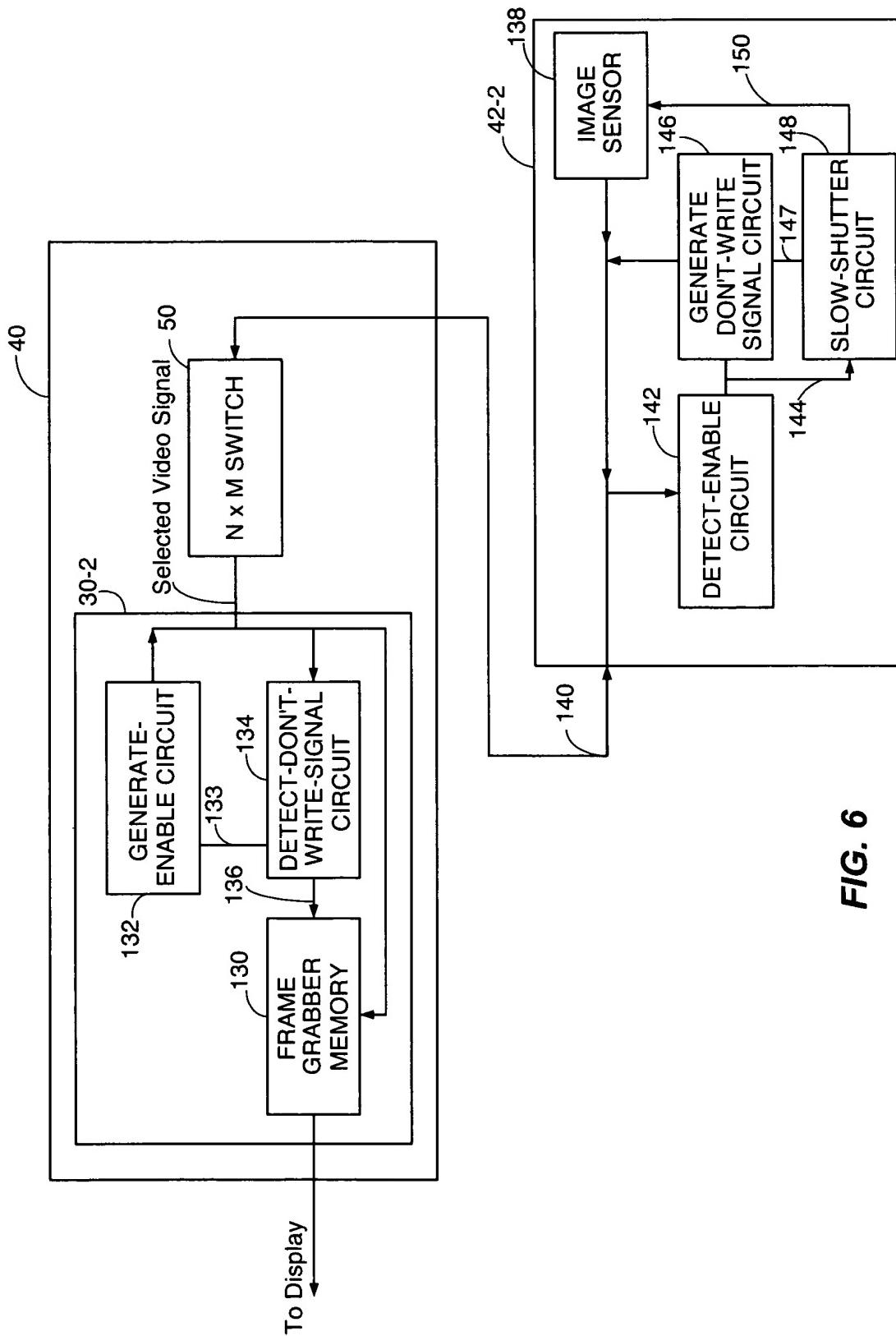


FIG. 5B
VIDEO SIGNAL WITH ENABLE PULSE





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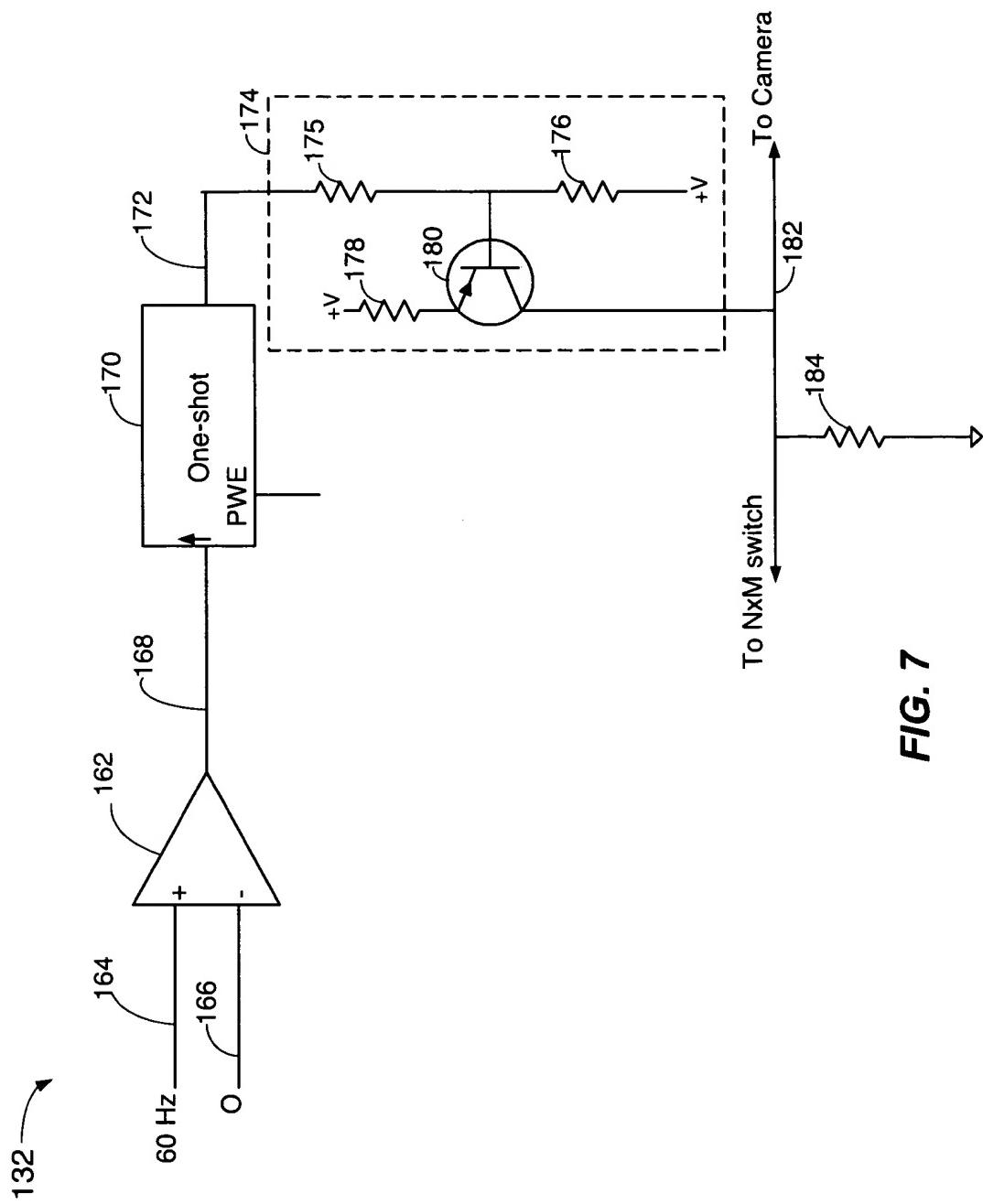
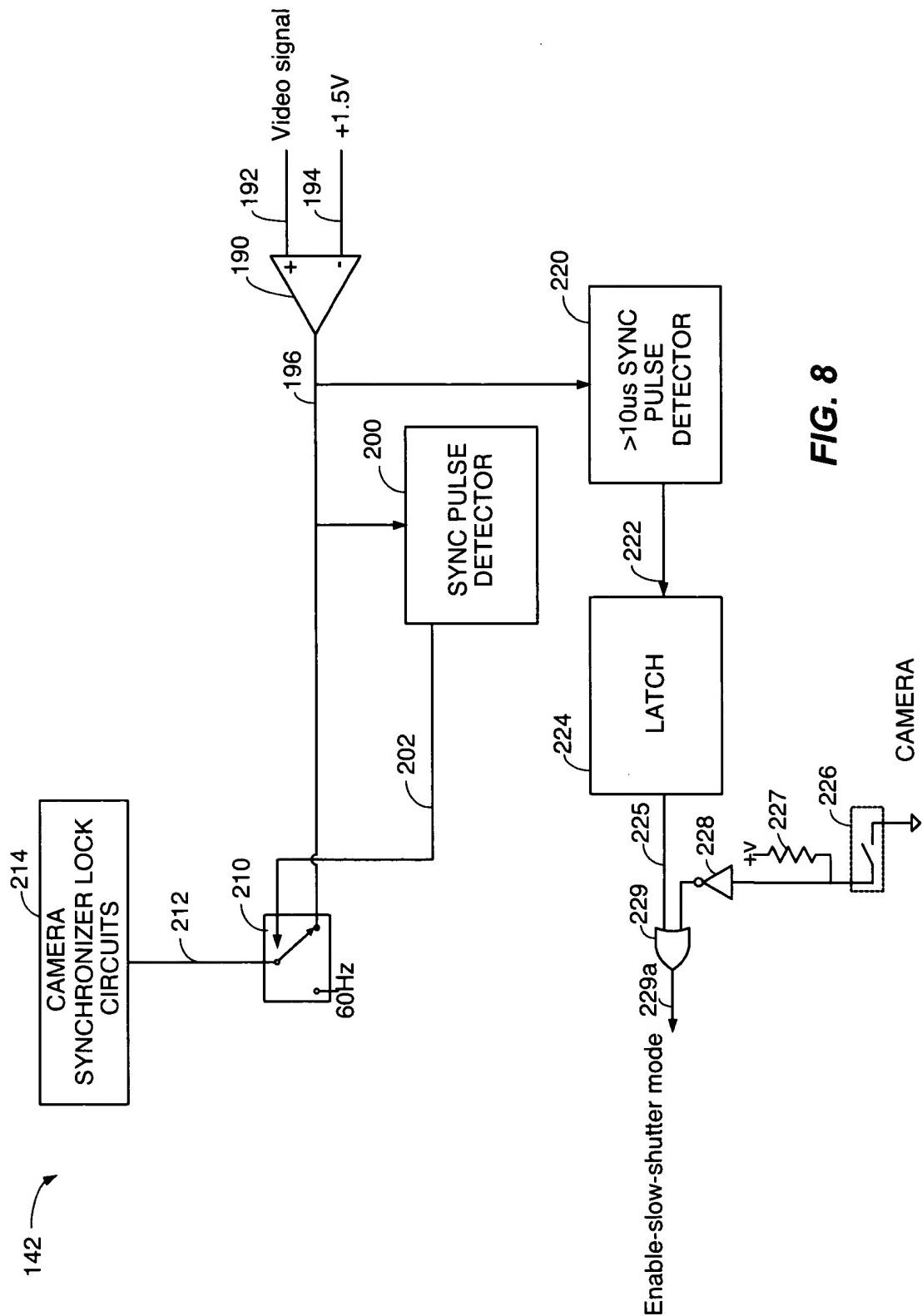
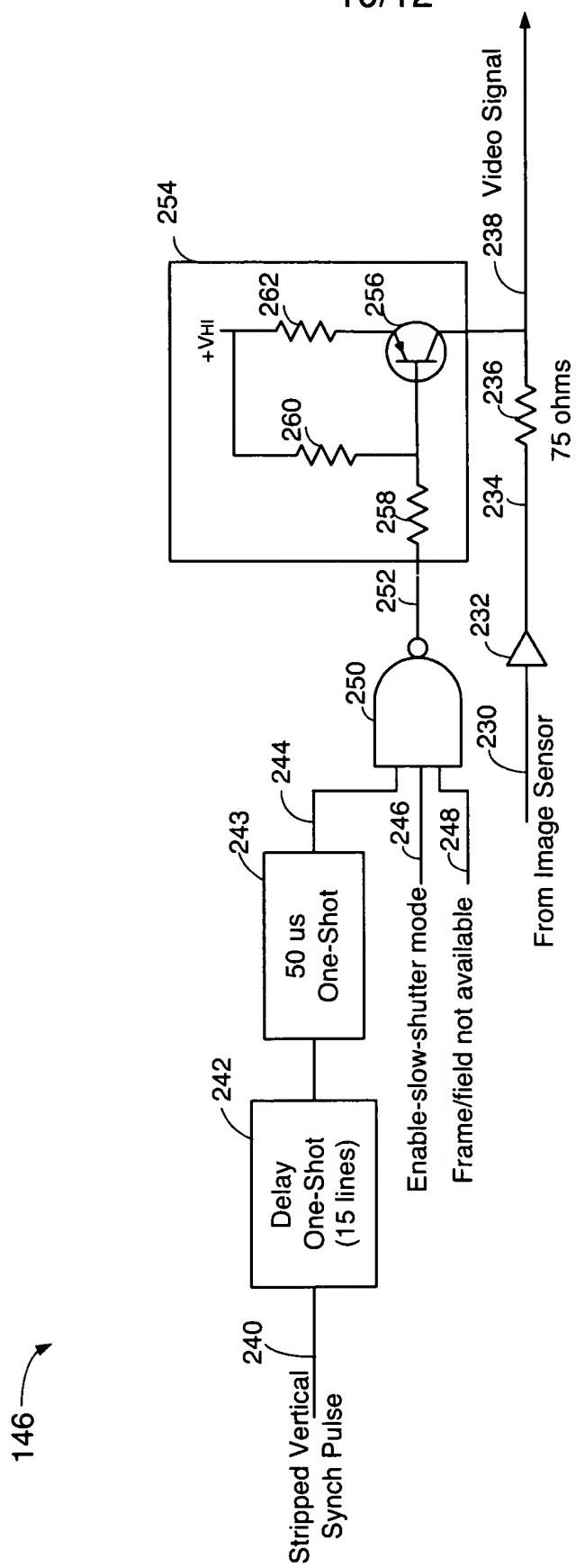


FIG. 7

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GENERATE DON'T WRITE SIGNAL CIRCUIT

FIG. 9

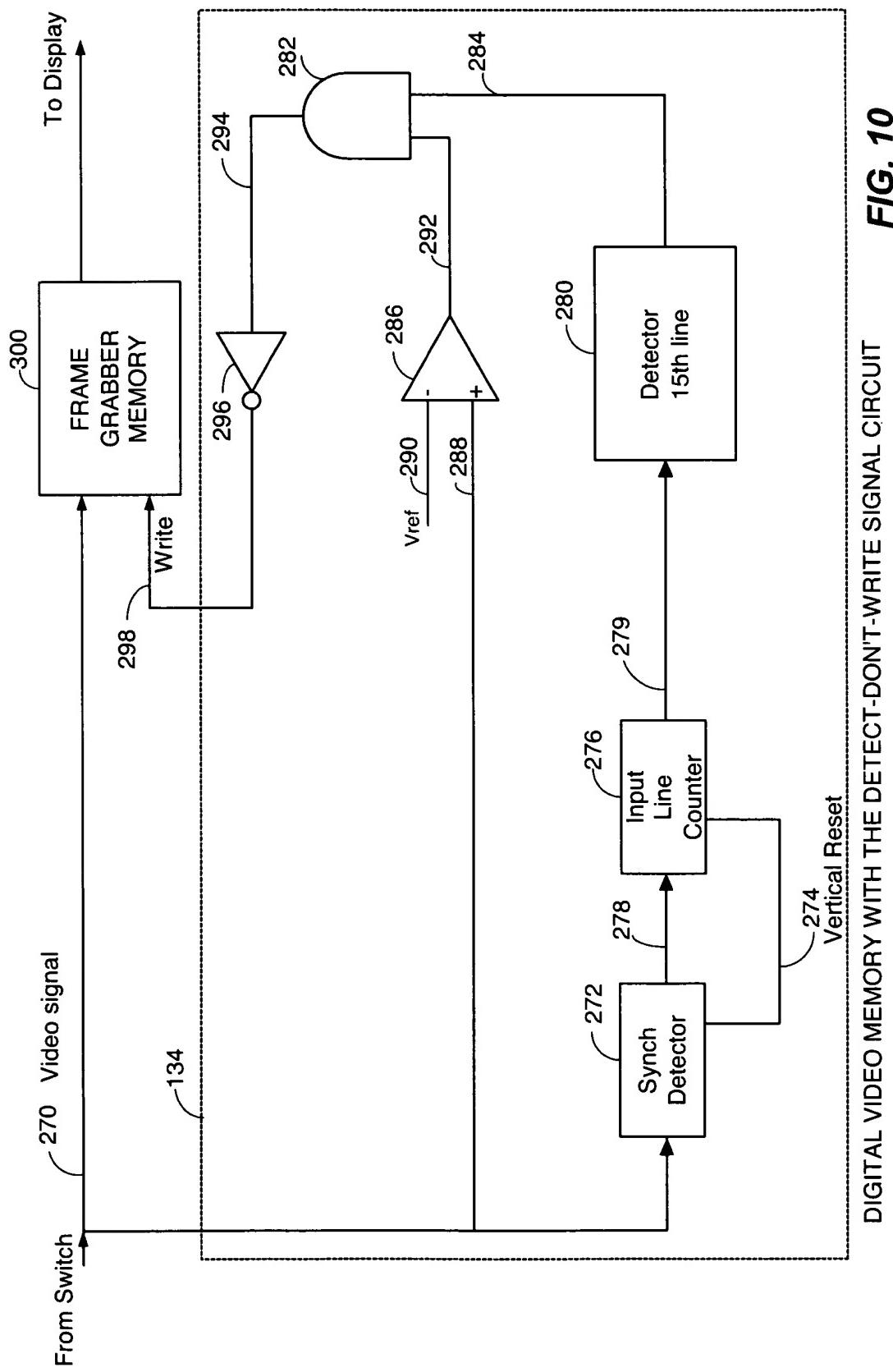


FIG. 10

DIGITAL VIDEO MEMORY WITH THE DETECT-DON'T-WRITE SIGNAL CIRCUIT

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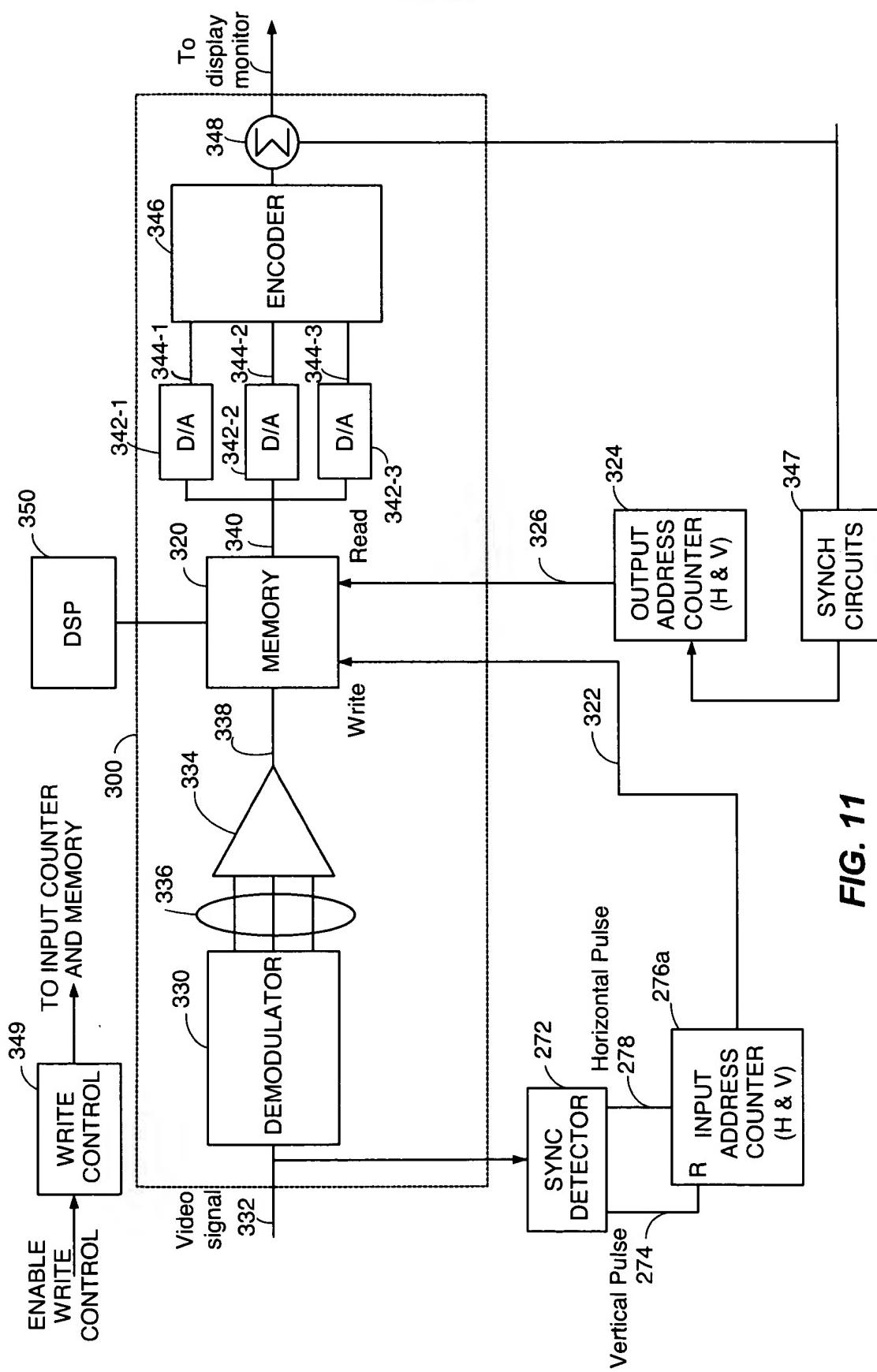


FIG. 11